Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 9 (Canceled)

10. (Currently amended) A hardware architecture for a core of a processor, comprising:

at least one unit for executing one of a logical or arithmetic operation; ~~and~~

an object-oriented data conversion unit for recognizing a type of an object and an object address, for external data, the data conversion unit being arranged to precede the unit for executing a logical or arithmetic operation, whereby the data conversion unit recognizes a type of an object based upon a type of information accompanying the object address and matches the type of an object and the object address before one of an operation is performed or a predetermined type of object is generated in the event of non-match; and

a microprocessor, including at least one register, the at least one register being divided into a first area for indicating the data or object type and into a second area for storing the data or object;

wherein an indication of the data type is stored in the first area when loading the piece of data to the register and when performing a logic or arithmetic operation on the data stored in the register, a data conversion is performed by the processor if required based on the indication stored in the register.

11. (Previously presented) The hardware architecture according to claim 10, wherein a memory location for the object address and a memory location of a register is respectively divided into a first area and a second area, whereby a type of the object is deposited in the first area.

12. (Previously presented) The hardware architecture according to claim 10, wherein the object-oriented data conversion unit is arranged to follow the unit executing a logical or an arithmetic operation.

13. (Previously presented) The hardware architecture according to claim 10, wherein the object-oriented data conversion unit is arranged to precede storing of the object in an external storage and a register file.

Claims 14 - 20 (Canceled)

21. (New) The hardware architecture according to claim 10, wherein the processor is configured for automatic index conversion based on the data type stored in the register together with the data when performing indexed addressing.